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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,621	12/05/2003	Yang Du	SC13135TC	9075

23125 7590 03/23/2005

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EXAMINER	
TSAI, H JEY	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,621	DU ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-25* is/are allowed.

6)☒ Claim(s) *26-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 26-28 are rejected under 35 U.S.C. § 102(a or e) as being anticipated by Mathew et al., 2003/0151077, newly cited.

Mathew et al. discloses a method of forming a semiconductor structure, which includes:

providing a substrate 12, fig. 1+ and para. 16+,

forming a semiconductor fin 18 on the substrate 12, the fin 18 having first and second sidewalls, see figs. 2+, para. 17+,

forming a layer of gate material 28 over the substrate 12 and the fin 18, the gate material 28 including a first portion adjacent to the first sidewall of the fin 18 and a second portion adjacent the second sidewall of the fin 18, fig. 3,

removing the layer of gate material 28 over the semiconductor fin 18 to leave a first gate 28 or 64/62 along the first sidewall and a second gate along the second

sidewall, wherein the first and second gates are electrically isolated, figs. 9,16 and para. 24, 31,

forming a symmetrical source and drain regions 52/54 relative to the first and second gates 28 or 64/62 such that a channel region will formed under first and second gate electrodes 28 or /64/62 during the operation of the semiconductor structure, wherein there exists a plane parallel to the substrate and wherein a portion of each of the source region, the drain region 52/54 and the channel region (adjacent to gate dielectric layer 26 of first and second sidewalls) are within the plane, figs. 9 and 16,

applying a first signal to the first gate 28 or 64/62, para. 24-25,

applying a second signal to the second gate 28 or 64/62,

forming source and drain regions (including pillar under 52/54), fig. 9, 16,

source contacts 52 are electrical connected (fig. 9, 16) and drain 54 contacts are electrically connected (fig. 9, 16), para. 24-25, 31-32.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 29 and 30 are rejected under 35 U.S.C 103 as being unpatentable over Mathew et al. as applied to claims 26 and 27 above, and further in view of Forbes 6,649,476, previously cited.

The difference between the references applied above and the instant claim(s) is: Mathew et al. teaches firming first and second vertical gate transistors but does teaches applying analog signal such as oscillator signal to the first and second vertical gate electrodes. However, However, Forbes teaches in col. 1, lines 14+ and fig. 11-17, CMOS circuit having first and second vertical gate electrodes 252 can be used in both digital signal (logic) and analog signal. And, analog signal is known in the art as time varying and oscillator signal in known as analog signal.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Mathew et al.'s process by applying analog signals to the first and second vertical gate electrode as suggested by Forbes because the structures can be used both in the logic and analog circuits, such multiplying the signal or video display devices.

Allowable subject matter

In view of amendment filed on Jan. 26, 2005, claims 1-25 are allowable.

Conclusions

Applicant's arguments filed on Jan. 26, 2005 have been fully considered but they are not persuasive. Newly cited reference clearly teach plane parallel to the substrate and wherein a portion of each of the source region, the drain region 32/34/52/54 and the channel region (adjacent to gate dielectric layer 26 of first and second sidewalls) are within the plane, figs. 9 and 16,

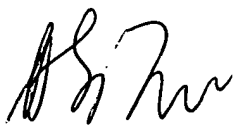
Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the customer service whose telephone number is (703) 308-4357 and Fax number (703) 872-9306.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone number for this Group is (703) 872-9306.

hjt

3/17/2005



H. Jey Tsai
Primary Examiner
Patent Examining Group 2800